AUTOTESTCON 2012 SEMINAR PROGRAM – MONDAY, SEPTEMBER 10, 2012

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ATE from A to Z

Instructor: Mike Ellis, Northrop Grumman Corp.

This seminar provides a complete overview of the world of ATE from a practical engineering and management viewpoint. Beginning by examining the ATE interfaces and their limitations, it offers managers and project engineers a quick and purposeful insight into the probable sources and causes of potential technical and management problems. Working from the interfaces, the seminar explores analog and digital test methods, examines the impact of new instrument technologies and covers the basics of switching systems and pin electronics. ATE software and languages will also be discussed**.**

No ATE seminar would be complete without a discussion of Commercial Off The Shelf hardware and software. A to Z will include a realistic, and entertaining examination of (COTS) application to the military ATE environment. Initially viewed as a panacea, it is now recognized that despite its many advantages, COTS is not a “free lunch”. Attendees are invited to visit “The Underside of the COTS Iceberg”, where they will travel through an actual COTS rehost of a complex ATE system. Take this opportunity to explore both sides of the COTS revolution, understanding both its opportunities and its challenges, while examining and learning from “other people’s mistakes”.

The seminar will conclude with a discussion of recent changes in DoD acquisition strategies and their potential impact on the future of ATE. Interoperability, net-centric operations, nanotechnology and smart sensors are high on OSD’s wish-list for new systems and will become an inherent part of the test and maintenance process. Explore DoD’s vision of the next generation of systems, where Test & Evaluation, Condition Based Maintenance, Training and Battle Damage Assessment become by-products of a distributed hierarchical, real-time information network. The future may be closer than you think!

TPS Management

Instructors: Mike Ellis, Northrop Grumman Corp, Ed Holland – NAVAIR (retired), Mitch Miller, Robins AFB

This four-part seminar is designed to cover the controversial and challenging issues of TPS Management from all perspectives; this session is a must for all industry and government TPS managers. As with the morning ATE session, it focuses on real world situations and explores areas of frequent problems.

Part I of the Seminar covers the tasks and challenges facing the government Acquisition Manager in preparing for, awarding and oversight of a TPS acquisition contract. It is based on the NAVAIR Generic OTPS RFP (aka Red Team). Ed Holland (NAVAIR retired) will cover the issues faced by the military in acquiring TPSs. He will discuss the NAVAIR OTPS Acquisition process, highlighting new requirements including those arising from the Systems Engineering Technical Review (SETR) process.

Part 2 of the seminar deals with the challenges a facing the TPS Developer. It summarizes the lessons learned from twenty years of TPS Development Management on over 1000 TPSs for all armed service branches. This part of the seminar will focus on planning and controlling a military TPS development project. Planning objectives will be those elusive goals, happy customer and a profitable project.

In Part 3 of the TPS Seminar, attendees will be provided in-depth insight into actual issues faced during TPS Acceptance Testing. This seminar section will lead attendees through an actual Acceptance Test, highlighting and discussing real-world problems and their resolution from the viewpoint of buyer and seller. Parts 2 and 3 will be taught by Mike Ellis of Northrop Grumman, and will draw upon over two decades of ATE and TPS consulting experience.

The final segment of the TPS seminar examines the maintenance role and responsibilities of the end product user. Mitch Miller from Warner Robins Air Logistics Center will provide the perspective of end-product maintenance and user insight of TPSs. This seminar segment will be based on "Depot 101, A Software Experience" course taught at the Airborne Electronics Division, Directorate of Maintenance, Robins AFB, GA as part of the "Blue Too" program. The course follows an actual TPS maintenance action from problem discovery through completion.

This unique four part seminar offers attendees the opportunity to "live" each of the TPS life cycle phases through the eyes of experts.. Along the way attendees will have the opportunity to examine the product and its challenges from four distinctly different viewpoints. They will explore the "pot holes" in the path to success and have the opportunity understand the implementation and impact associated with effective, on-time TPSs delivered within budget

Design for Built-In (Self) Test

Instructor: Louis Y. Ungar, A.T.E. Solutions, Inc.

With increased circuit complexity in recent years *almost* every test approach has had to settle for lower fault coverage, more difficulty in diagnoses and all at greater costs. The notable exception is Built-In Test (or Built-in Self Test, BIST) or as it is often called, embedded test. BIST is a phenomenon that capitalizes on greater circuit complexity (intelligence), better fault isolation from a hierarchical allocation of tests, and does not rely on costly external automatic test equipment (ATE) and test program sets (TPS). The inclusion of boundary-scan circuitry in increasing numbers of today’s chips has made circuit testability more readily available at board and system levels. Inclusion of BIST structures in less, but significant number of chips, has made it possible to invoke chip-level tests even during normal operation. These two developments, already in place for the past several years, and greatly accelerated in the past few years, have not only made component-level, board-level and system-level BIST possible to run after system deployment, but it has also made hierarchical BIST feasible. With hierarchical BIST, diagnostic resolutions can be greatly improved, and self-testing, self-diagnostic, even self-prognostic systems are achievable.

This seminar is aimed at professionals in all areas of support, including reliability, maintainability and logistics, as well as engineers and managers from design, test, and quality assurance.

The course will discuss how test issues can be effectively dealt with at the design level by creating testable circuits. Using boundary scan (JTAG/IEEE-1149.1) techniques, as well as mixed signal (IEEE-1149.4) and AC-coupled nets (IEEE-1149.6) testability standards, it is now possible to gain chip-level access through a system-level connector. Combining these techniques with internal scan and BIST structures, attendees will learn how to design tests into a circuit. Utilizing BIST structures that are increasingly embedded into chips, or programmed into field programmable gate arrays (FPGAs) through JTAG in-system programming (ISP), a larger percentage of the circuit can be made testable. The cost of using such techniques is on the decline, while the benefits that can be gained are ever greater. While software approaches to built-in test are mature and widely accepted at the system-level, project managers need to consider the added rewards of hardware BIST. It can improve diagnostics, reduce the expense of ATE and of test program set (TPS) development, and offer a platform for prognoses. In some circuits, such as memories, BIST gives way to built-in repair analysis, and even built-in self repair.

This course will provide attendees with the understanding they need to plan system designs for test and for built-in tests. The course will also discuss how these techniques affect supportability issues, including reliability, availability, operational readiness and false alarms.

Diagnostic Modeling and Application Development

Instructors: Dr. John W. Sheppard, Montana State University; Timothy J. Wilmering, The Boeing Company

This seminar provides an overview of traditional and more recent approaches to system-level diagnosis and prognosis. The emphasis is placed on different system modeling approaches and the algorithms that can be applied using resulting models. The seminar is organized in three parts:

Part 1: The Diagnostic Landscape. The seminar will begin by reviewing the basic issues and challenges in system diagnosis and prognosis. Fundamental terms and concepts of fault diagnosis will be presented with focus being given to historical approaches and the needs from the perspectives of the Department of Defense. Recent initiatives such as DoD ATS Framework, NxTest, ARGCS, and ATML will also be introduced.

Part 2: Diagnostic and Prognostic Algorithms. In the second part of the seminar, diagnosis will be defined within the context of classification problems. Central to this part of the seminar will be a continuing discussion of how one handles uncertainty in the diagnostic and prognostic process; therefore, the primary focus of this part will be recent developments in applying Bayesian techniques to fault diagnosis and prognosis. Prognosis will be related to the diagnosis problem in the context of "predictive" classification, and Bayesian extensions, such as hidden Markov models and dynamic Bayesian networks will be discussed.

Part 3: Health Management Information Integration. The third part of the seminar will focus on information integration issues in developing health management systems. The discussion will focus on using formal models, called ontologies, to define the semantics of the required information and then focus on processes for maturing diagnostic applications as maintenance information is collected. Emerging standards being developed within the IEEE related to diagnostic and maintenance information will be reviewed. The seminar will end by reviewing the state of the art and providing an overall assessment of how well diagnosis and prognosis can be performed.
Throughout the discussion, the seminar will draw upon experiences of the instructors and participants to highlight issues related to diagnostic development within defense and commercial environments.

Familiarization and Use of IEEE Std 1641-2004 (IEEE Standard for Signal and Test Description)

Instructors: Chris Gorringe & Matt Cornish, EADS Test Engineering Services, (UK) Ltd.

The IEEE standard for Signal and Test Definition (IEEE 1641) is part of the DoD ATS Technical Framework, under consideration for inclusion in the DoD DISR and its use is UK MoD procurement policy for all new TPS and ATS. IEEE 1641 is also a key element within IEEE 1671 ATML, providing signal definition for Test Description and Instrument Description. Beyond defense, 1641 is also gaining interest within the semi-conductor test industry.

This seminar provides an introduction to IEEE 1641, for those likely to be involved with future & re-host test systems for the DoD or MoD. The seminar is especially targeted at those who are responsible for specification, acquisition, development, or implementation of test requirements, such as Project and ILS Managers. It also includes valuable information for those who are responsible for the design and operation of automatic test systems, such as team leaders and technical leads.

The first part of the seminar covers essential concepts, with the message that 1641 is about reducing the whole-life costs of maintaining test requirements & systems. In particular, how the standard provides a mechanism for achieving portable and repeatable test requirements that are based upon signal requirements defined with mathematical rigor. It affords an understanding of the principles & functions of the standard and explains the importance of the role of the standard in the development of test systems & requirements.

The second part of the seminar discusses various practical issues, drawing upon the experience of the presenters. These include how items such as measurements, tolerances and more complex signals (e.g. sweep signals) may be defined and implemented. The seminar demonstrates procedures for defining true portable signal requirements and shows how 'specific' or special-to-type ATLAS nouns can be defined, thus showing that IEEE 1641 and can be used to enable TPS re-host and interoperability.

VXI, PXI, IVI, LXI and AXIe Standards Improve ATE Systems Design

Instructor: Bob Helsel, currently managing the following T&M consortia: VXIbus Consortium, PXI Systems Alliance, IVI Foundation, LXI Consortium, and AXIe Consortium.

The VXIbus architecture was introduced 25 years ago, and is currently a well-established architecture used extensively in military, aerospace and commercial applications. However, many test engineers have no personal experience with it, or would like to brush up on its basics, as it will be around for another 10-20 years. We will cover the approval in 2004 of the VXI-1 Rev 3.0 spec, which again doubles the backplane speed to 160MB/s. And we will cover the approval of VXI 4.0 and its improvements in speed and flexibility. VXIplug&play standards are the software equivalent to the VXI hardware specifications, and are the definition to which all VXI drivers are now written. This software standard has formed the bedrock for many other software developments, such as Interchangeable Virtual Instrument (IVI) drivers.

PXI is a newer, more compact, faster hardware standard based on CompactPCI. It applies the same extensions to CPCI that VXI did to VME. This modular instrument standard rapidly gained acceptance and can be viewed as a companion standard to VXI, (or by some as a replacement). This 15-year-old hardware standard will be discussed in detail, as will its expected impact on

the market. An update will be provided on Enhanced PXI specifications and their implementation, including Low Power Chassis. PXI Express and PXI MultiComputing will be explained with a review of PXI express products and their potential applications.

The Interchangeable Virtual Instrument (IVI) software standard, which has been extensively revised and expanded, will be covered with the latest information available. The IVI Foundation was founded in 1998 and incorporated in 2001. The purpose of the IVI Foundation is promoting specifications for programming test instruments that simplify interchangeability, provide better performance, and reduce the cost of program development ***and maintenance.*** IVI Instrument drivers have been available for about 11 years. New Specifications for Digital Test, Counter/Timer, and Signal Oriented test plus LXI triggering and sync will also be discussed.

The LXI Consortium is about 7 years old now, and was formed to standardize the way instruments can be connected and controlled via the Internet in a Local Area Network. Extensions for discovery, triggering and synchronization, browser interface, initialization, and programming are all part of the extensions being considered in this standardization effort. We will introduce the latest release of the LXI Specification as well as the introduction of new LXI compliant products that are now available.

An emerging test and measurement standard called AXIe, AdvancedTCA eXtensions for Instrumentation (http://www.axiestandard.org/), is expected to find wide acceptance within the Automatic Test Equipment community as it offers many key benefits. It is expected that a large number of COTS (commercial off-the-shelf) signal conditioning, acquisition and processing modules will become available from a range of different suppliers. AXIe uses AdvancedTCA® as its base standard, but then leverages test and measurement industry standards such as PXI (http://www.pxisa.org/), IVI (http://www.ivifoundation.org/), and LXI (http://www.lxistandard.org/), which were designed to facilitate cooperation and plug-and-play interoperability between COTS instrument suppliers. This enables AXIe systems to easily integrate with other test and measurement equipment. AXIe's large board footprint, available power and efficient cooling to the module payload allows high density in a 19" rack space, enabling the development of high-performance instrumentation in a density unmatched by other instrumentation form factors. Channel synchronization between modules is flexible and provided by AXIe's dual triggering structures: a parallel trigger bus, and radially-distributed, time-matched point-to-point trigger lines. Inter-module communication is also provided with a local bus between adjacent modules allowing data transfer rates up to 10 Gbits/s in each direction, for example between front-end digitizer modules and DSP banks. AXIe is a next-generation, open standard that extends AdvancedTCA® for general purpose and semiconductor test.

This comprehensive update on the development of commercial standards for the ATE community should not be missed by anyone concerned with current and future ATE systems design and integration.

System Software Testing Using DO-178B and DO-254

Instructor: Mark Everly, President, TSS Inc.

As systems increase in complexity they increasingly rely on software to provide much of their functionality. Hardware testing methods are well established, but standardization of software testing methods has lagged its hardware counterpart. ARINC Standard DO-178B seeks to close this gap. The purpose of DO-178B is to "provide guidance for determining, in a consistent manner and with an acceptable level of confidence, that the software of airborne systems and equipment comply with airworthiness requirements." While focusing primarily on flight-critical software, DO-178B methods are rapidly becoming the *de facto* standard for all software testing. This seminar addresses automated testing methodologies that achieve complete and consistent results to fulfill the purpose of DO-178B.

When implemented properly, automated testing can effect up to a 25% efficiency increase during initial product development and over 50% for subsequent product enhancements. When implemented improperly, automated testing can lead to excessive budget and schedule overruns. This seminar will explore effective automated testing paradigms that fulfill the purpose of DO-178B and methods that ensure success from project onset. To achieve these goals, the areas of DO-178B that typically affect the largest amount of budget and schedule overrun will be addressed and plans to mitigate these areas will be presented.

ATS Considerations for New Testing Technologies

Larry V. Kirkland WesTest Engineering, Corp. R. Glenn Wright GMA Industries, Inc.,

This seminar addresses the introduction of new testing technologies into today's automatic test systems (ATS) in an effort to fulfill current and future test requirements for printed circuit boards (PCBs). The increasing gate density of electronic components, combined with new levels of functionality equal to entire system levels of just ten years ago, call for new approaches to testing that stretch the imagination and cry out for new definitions of testing philosophies. An interface is no longer limited to direct connections to card-edge connectors and test points, but comprises the complete geometry of the PCB accessible across the entire spectrum from DC to the terahertz region and beyond without relying simply on physical connections. Sensors used for test can range in scale from centimeters to nanometers, both external and internal to the PCB, and are able to observe electrical, chemical, physical and other phenomena previously not capable of being measured. Sensor data processing and failure event interpretation has entered into a new realm of sophistication and complexity to detect and identify not only PCB components (electrical, electromechanical, mechanical and the PCB itself) that have failed, but are likely to fail in the future. More interestingly, the question of what comprises test requirements may now extend beyond specifically what the UUT is supposed to do and when it does it, given a particular set of stimulus, to how and why it does what it does.

Methods of UUT interrogation and observation of circuit board and component behavior via direct connection, wireless, and passive means are discussed. An overview of existing and advanced sensor technologies relating to functionality, test capabilities and limitations, current state of the art, and cost is provided covering: analog and digital, thermal and infrared, electromagnetic emissions, laser vibrometry, X-ray, terahertz, and gas and materials sensors. Hardware and software issues are also considered, addressing such topics as sensor integration and data fusion, visualizing test processes and analyzing test results, robotics as a means of enhanced UUT access, and integration of new technology into existing legacy ATS.